ISSN: 0975-8585

Research Journal of Pharmaceutical, Biological and Chemical Sciences

Analysis of Mac Unit Using Vedic Multiplier and Sklansky Adder.

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ABSTRACT

Digital signal processing is the one of the technologies in highly growing application areas like wireless communications, audio and video processing. In digital signal processor one of the main blocks is Multiplier and Accumulator (MAC) Unit. In this paper, the Multiplier Stage is done by using Vedic multiplier with Parallel-Prefix adder and the delay performance with ripple carry adder is compared. These days Parallel-Prefix adders are the commonly used adders due to the high speed computation properties. The speed of operation is achieved by the nature of Vedic multiplier. This paper presents the design of MAC Unit using Sklansky adder (Parallel Prefix adder). The Verilog HDL Code is use to design MAC Unit and the simulations are performed using the Xilinx ISE tool 10.1.

Keywords: Mac unit, sklansky adder

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ISSN: 0975-8585

INTRODUCTION

Digital multipliers are the core mechanism of all digital signal processors. Speed of DSP is largely determined by the speed of its multiplier unit. Multiplier accumulator (MAC) operation is a commonly used process in various digital signal processing application. MAC unit operation is the key operation of most of the high performance microprocessors, FIR filters, etc.; normally a MAC unit consists of multiplier and accumulator part, where the accumulator stores the previous multiplication products. In multiplier stage it has three main stages. They are partial product stage, summation stage and final adder stage [9],[11]. In these three, final adder stage is responsible for speed and the delay. An efficient MAC unit high speed, low power, area and accuracy are very important. Critical path delay is the vital factor in determining the speed of the multiplier. Multiplier is not only the high delay block but also a major source of power dissipation [10]. So, the aim is to minimize the power consumption. It is of great consideration to reduce the delay by using an array of delay optimization. In this paper, in multiplier stage the design is done by using Vedic multiplier and the adder part is design by using various adder methods and their performances are compared. In adder stage Ripple carry adder [1] and Sklansky adder are used to design the MAC unit and their performances are analysed. In this work, two MAC Unit are designed. The first unit consists of Vedic Multiplier with Ripple Carry adder and second MAC unit consists of Vedic Multiplier with Sklansky adder (parallel prefix adder).

VEDIC MULTIPLIER

The formulate "Vedas" means understanding has derivational significance as standard and immeasurable storehouse of all knowledge. Vedic mathematics is based on 16 formulas (sutras) and 13 Upa sutras (corollaries) [5],[1]. All mathematical problems are solved mentally with these sutras. Vedic multiplier is different from conventional multiplier. The Vedic multiplier is based on the Vedic multiplication formulas. These formulas are designed for the multiplication of two numbers in decimal numbers systems [6],[12]. The main goal of Vedic mathematics is to be able to solve complex calculation by simple mechanism. The formula being very short their practical application becomes very simple. The advantage of Vedic multiplier, it can be easily realized on hardware. In this paper, the Urdhva Tiryagbhyam Vedic sutra is used to design the multiplier stage.

URDHVA TIRYAGBHYAM

Urdhva Tiryagbhyam sutra, Urdhva means vertically up/down and Tiryagbhyam means left to right or vice versa [1]. The advantage of Vedic multiplier is, if the number of bit increases, the gate delay and the area increase very slowly as compared to other multipliers. So it consumes less time, space and power efficient. Urdhva Tiryagbhyam algorithm is a wide-ranging multiplication formula appropriate to all types of multiplication.

Regard as multiplication of two decimal numbers (21×32) in Figure 2.1. In the beginning the LSB of equally the numbers are multiplied and added with earlier carry. This generates one of the bits of the bits of the result and a carry. In the subsequently step the LSB and the bit next to LSB are multiplied in a diagonally manner and the earlier carry is added with it. The similar process of vertical and crosswire multiplication is continual to get the final answer [6].

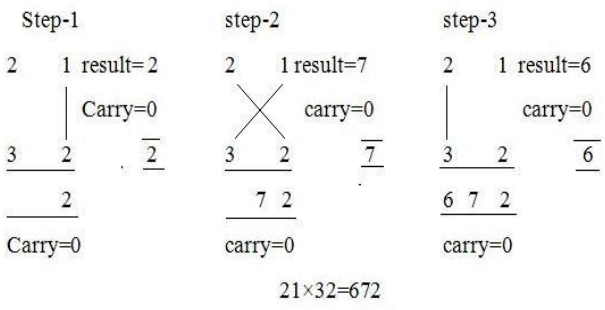

Figure 2.1 Urdhva Tiryagbhyam multiplication of two decimal numbers [6].

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PARALLEL PREFIX ADDER

Parallel prefix adders are identified to have the greatest concert in VLSI designs. Prefix means the effect of the operation is depends on the initial inputs and parallel defines that it involves the execution of an operation in parallel. This can be done by segmentation into minor piece that are compute in parallel. This adder has bestperformance in VLSI technology. Parallel-prefix adders are more favourable in terms of speed due to the convolution O (log_2N) delay during the carry path compared to that of other adders [2].

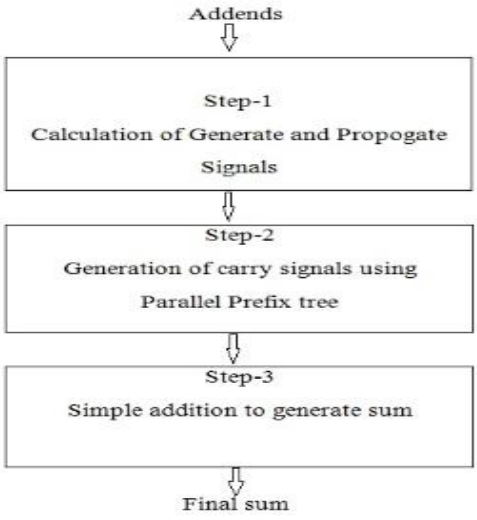

Figure 3.1 Addition Procedure Using Parallel Prefix tree structure [7].

The Parallel prefix addition is ended in three steps, that shown in Figure 3.1. The first step is parallel prefix addition is to compute the Propagate and generate signals. By using these type of generate and propagate signals, carry input signals of all bit addition are generated, carry input signals are used in final addition to produce the sum output [7]. In this paper the Sklansky adderis used in the multiplier stage.

SKLANSKY ADDER

The Sklansky adder is also the tree adder family. Difference between the other adders and Sklansky adder is prefix network. It has dot operators. The square box is dot operators and the gray square box is empty dot operators and the Triangle refers to the buffer operation. The Figure 3.2 shows the structure of Sklansky adder [4].In this Sklansky adder it consists of three cells. They are Black cell, Gray cell and Buffer cell. The Black cell, shown in Figure 3.3 performs AND-OR-AND logic operation. The Gray cell shown in Figure 3.4 perform AND-OR logic operation[3].

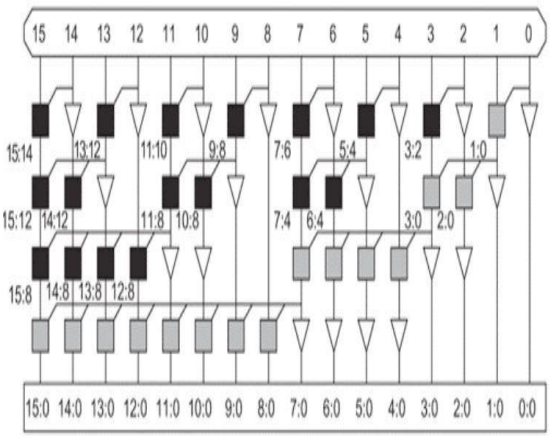

Figure 3.2 Structure of Sklansky adder[4]

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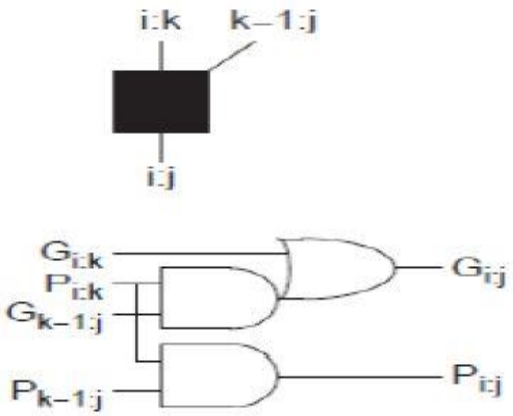

Figure 3.3 Black cell [3]

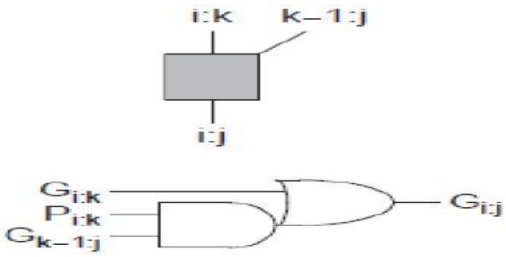

Figure 3.4 Gray cell [3]

The Sklansky type of tree adder is chosen due to its low power consumption than that incurred by other tree adder structures. The advantage of this adder is it has minimum logic levels and wiring tracks compare to other tree adders.

VARIOUS MULTIPLIER ARCHITECTURES

In proposed multiplier consists of 8-bit Multiplier and 8-bit adder stage. In multiplier stage 8-bit multiplier performs 4×4 Vedic multiplication operation [1]. Let us assume A and B is the 8-bit input. A= A0 A1 A2 A3 A4 A5 A6 A7 and B= B0 B1 B2 B3 B4 B5 B6 B7. Let's divide A and B each has two part A(0-3) and A(4-7) like that B(0-3) and B(4-7). This input is given to the 4×4 Vedic multiplier in A×B manner. Therefore, there are fourVedic multiplier (M1, M2, M3 and M4) are used for 8-bit multiplier. Each multiplier stage gives two pair of 8-bit output. The outputs of 4×4 Vedic multipliers are added accordingly to obtain final product. In this paper two adders are compared in multiplier stage. i.e.,(i) Vedic multiplier with 8-bit ripple carry adder [1] have shown in Figure 4.1 and (ii) Vedic multiplier 8-bit Sklansky adder shown in Figure 4.2.

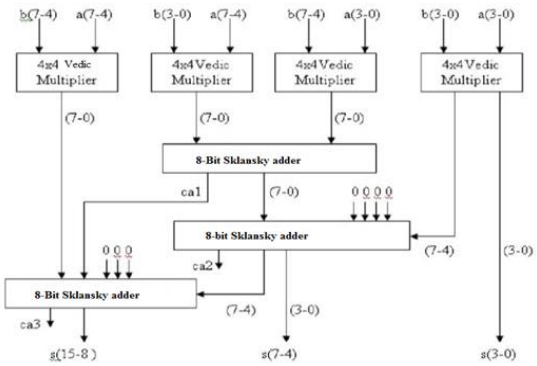

Figure 4.1 Block diagram of Vedic Multiplier with Ripple carry adder [1]

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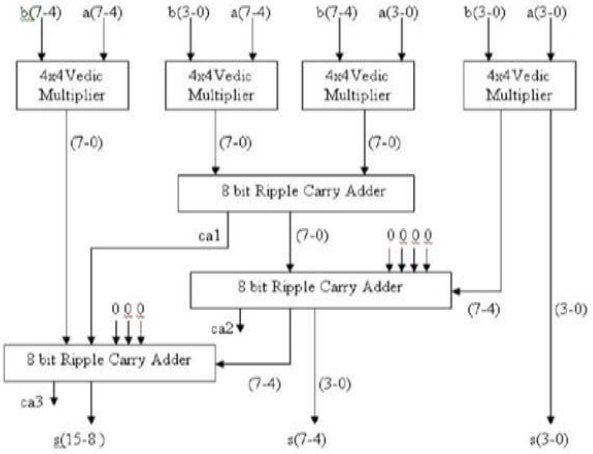

Figure 4.2 Block Diagram of Vedic Multiplier with 8-bit Sklansky adder

PROPOSED MAC UNIT ARCHITECTURE

Proposed MAC Architecture is designed by using different adders. They are MAC Unit using Ripple Carry adder and MAC unit using Sklansky adder, the block diagram of proposed one is shown in figure 5.1. In the multiplier stage they produce 16-bit output. That 16-bit output is applied to the 16-bit adders input. To design the MAC unit 16-bit adders are used i.e., Vedic multiplier with 8-bit ripple carry adder output is given to the 16-bit Ripple carry adder input. Vedic multiplier with 8-bit Sklansky adder output is given to 16-bit Sklansky adder input. This 16-bit adder gives the 16-bit input to the accumulator. Accumulator Part gives the output. In this proposed MAC unit, accumulator operation is done by using D-flip flop. Generally, Accumulator part is act as a memory element. Then the proposed MAC Architectures are compared by their performance.

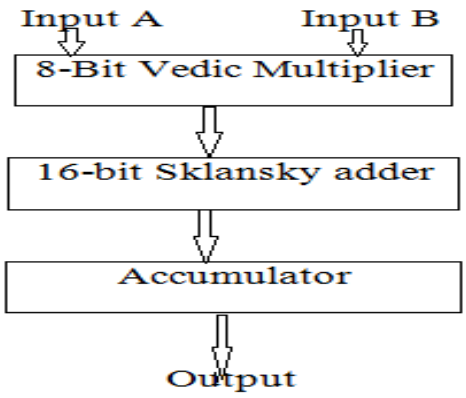

Figure 5.1 Block Diagram of Proposed MAC Unit using 16-bit Sklansky adder

RESULT AND DICUSSION

In this work, multiplier stage and MAC unit are designed using Verilog HDL in Xilinx ISE 10.1 tool and Simulations are performed using Modelsim Altera-6.5 simulator. The Performances are compared for different multiplier and analyzed the delay of multiplier. Then the MAC unit are designed using these multiplier and the delay performance are compared.

ISSN: 0975-8585

Performance analysis of Multiplier Stage

Table.1 Delay Comparison of Multiplier stage

DELAY COMPARISON TABLE			
METHOD	LOGIC	ROUTE	TOTAL DELAY
Vedic Multiplier with 8-bit Ripple Carry adder	15.717ns	10.136ns	25.853ns
Vedic Multiplier with 8-bit Sklansky adder	14.963ns	9.351ns	24.314ns

Performance Analysis of MAC Unit

Table.2 Delay Comparison of MAC Unit

DELAY COMPARISON TABLE			
METHOD	LOGIC	ROUTE	TOTAL DELAY
MAC Unit using 16-bit Ripple Carry Adder	17.759ns	11.976ns	29.735ns
MAC Unit using 16-bit Sklansky Adder	16.907ns	11.074ns	27.981ns

SIMULATION RESULT OF MULTIPLIER

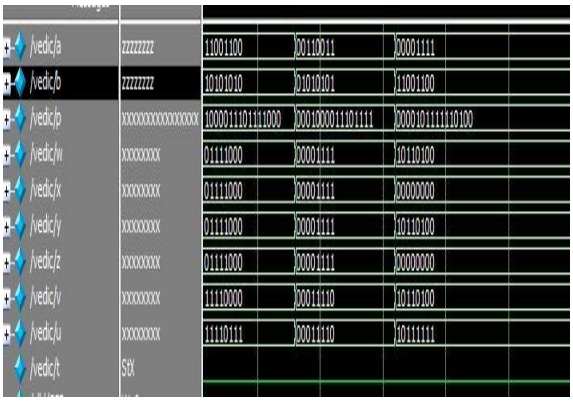

Figure 6.1 Simulation Result of Vedic Multiplier with 8-bit Ripple Carrey Adder

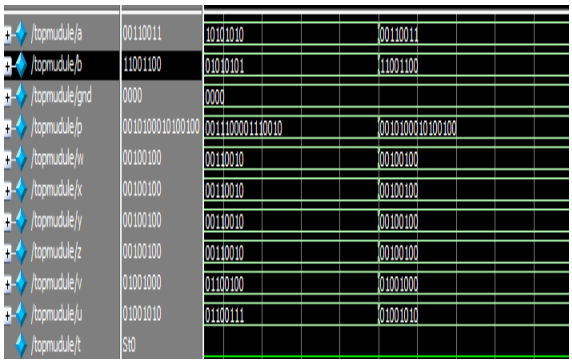

Figure 6.2 Simulation Result of Vedic Multiplier with 8-bit Sklansky adder

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SIMULATION RESULT OF MAC UNIT

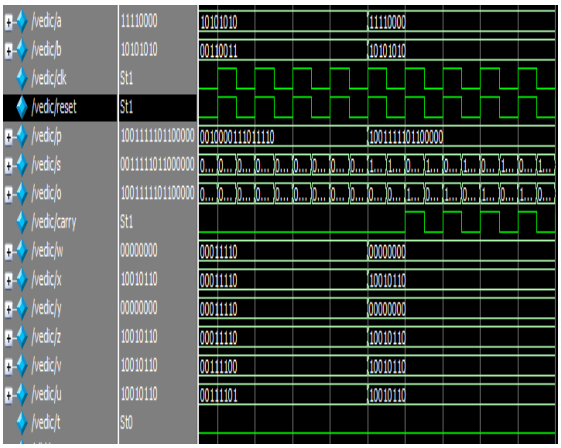

Figure 6.3 Simulation Result of MAC Unit using 16-bit Ripple Carry adder

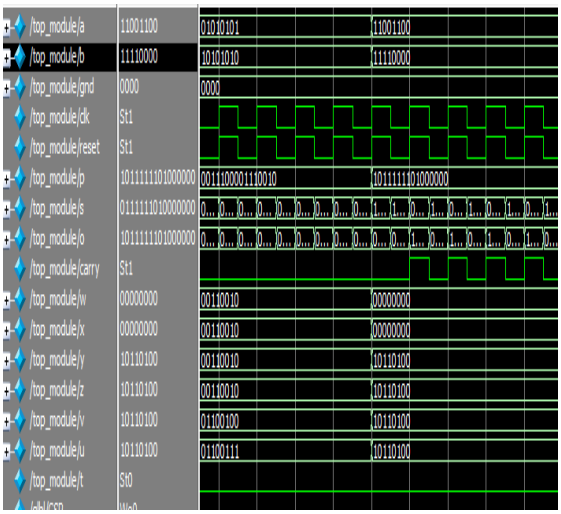

Figure 6.4 Simulation Result of MAC Unit using 16-bit Sklansky adder

RTL SCHEMATIC OF MULTIPLIER STAGE

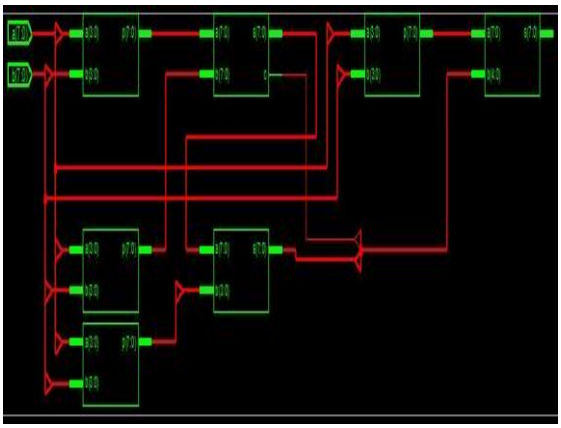

Figure 6.5 Schematic design of Vedic multiplier with 8-bit Ripple Carry adder

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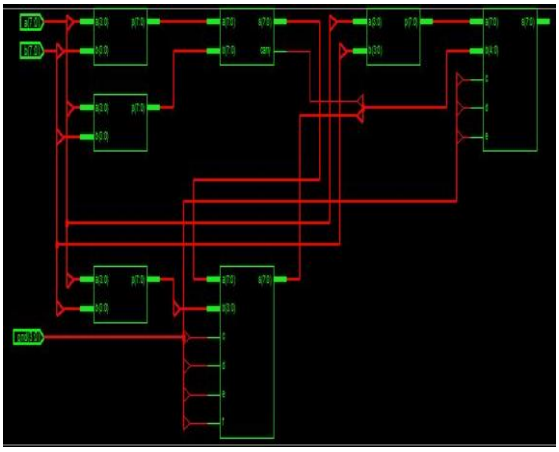

Figure 6.6 Schematic design of Vedic multiplier with 8-bit Sklansky adder

RTL SCHEMATIC OF MAC UNIT

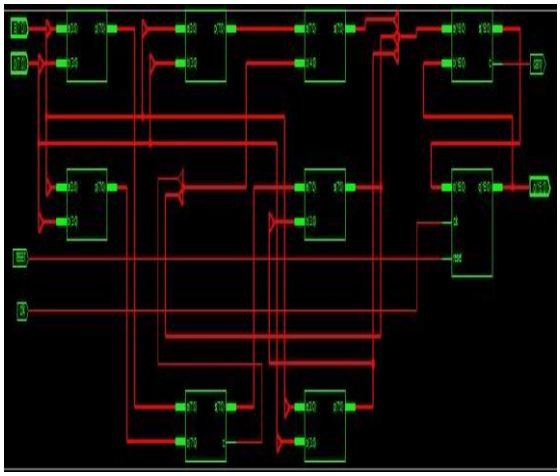

Figure 6.7 Schematic design of MAC Unit using 16-bit Ripple Carry Adder

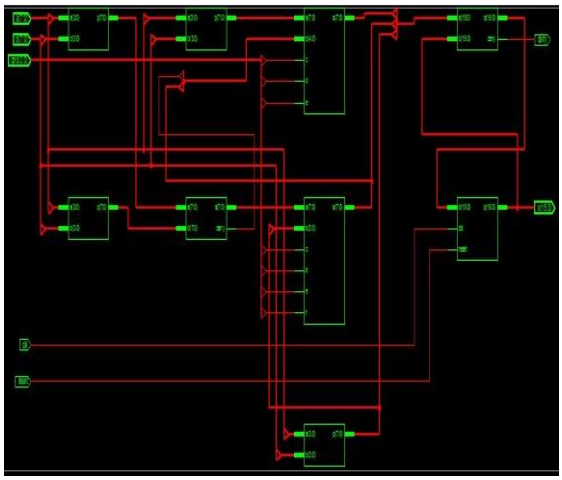

Figure 6.8 Schematic design of MAC Unit using 16-bit Sklansky Adder

CONCLUSION

This paper presents proficient multiplier-"Urdhva Triyagbhyam sutra" based Vedic multiplication with Sklansky adder. The designs and performances of multiplier stage and MAC Unit using various adders are

compared. On comparing the performance of multiplier and MAC unit designs, Sklansky adder used MAC Unit give minimized delay which mechanically increase the performance of the MAC Unit.

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