ISSN: 0975-8585

Research Journal of Pharmaceutical, Biological and Chemical Sciences

A Survey on Different Floorplanning Techniques.

Abinaya S[1]* and Saravanan S[2].

[1]m.Tech Vlsi Design, Sastra University, Thanjavur, Tamil Nadu, India-613401.
[2]assistantprofessor , School Of Computing, Sastra University, Thanjavur, Tamil Nadu, India-613401.

ABSTRACT

A survey on physical design of the floorplanning in VLSI is discussed using different optimization techniques for better performance, good reliability and yield of the VLSI chip. The comparison of Genetic Algorithm (GA), Particle Swarm Optimization (PSO) and Firefly Algorithm (FA) are discussed for analysing the better performance. Particle Swarm Optimization is used for multi objective floorplan. For representation B* tree representation and Modified Corner List algorithm are compared and performance are identified. From this identification, MCL has more flexibility and less computational complexity.

Keywords: Particle Swarm Optimization, Ant Colony Optimization, Corner Block List, VLSI floorplan, MCNC benchmark circuit.

Corresponding author

ISSN: 0975-8585

INTRODUCTION

Floorplanning is the initial physical design step of VLSI chip. It should estimate the good reliability, yield, area and performance and it is the crucial part of the design. In VLSI floorplan each and every module should not overlap each other. The main goal of the physical design of floorplan is to optimize the chip area and obtain minimized wirelength. In the Physical design even the small problem makes the huge issue which increases the temperature. If the temperature increases power consumption will be high and decreases in the overall performance of the chip. Due to high temperature the function of the chip is low.

It is an NP hard problem and in the floorplanning more number of evolutionary algorithm are used for better solutions. The algorithms such as Genetic Algorithm (GA), Particle Swarm Optimization (PSO), ArtificialBee Colony (ABC) and etc. Genetic Algorithm is used to tackle the NP hard problem in VLSI floorplan. Particle Swarm Optimization is developed from birds flocking and even from human behaviour. Hence PSO is population based algorithm and PSO finds the optimal solution. Floorplanning also considers the IO structure and aspect ratio of width and height of the VLSI chip. Imbalance floorplanning increases the dead space of the chip and the routing and placements depends on floorplanning.

The evolutionary algorithm is used for less chip area and less interconnects. Some techniques are used for initialization and representation of the each modules in the floorplan. The techniques called B*tree algorithm, Modified Corner List algorithm (MCL) and O tree algorithm. MCNC benchmark circuits are used to analyse the performance of the algorithm.

RELATED WORKS

Temperature awareness is achieved in this paper [1] using Ant Colony Optimization (ACO) in VLSI floorplanning and it also focused on area optimization. Different methods of optimization technique were implemented to reduce temperature and area using MCNC circuits. Ant Colony Optimization technique is better when compared to Simulated Annealing (SA) with low latency and high throughput.

Discrete Particle Swarm Optimization algorithm was utilized in this paper [2] to achieve arbitrary area and minimization of the wire length interconnections. In proposed system PSO was employed with the integer coding depends on the module number and some value of acceleration co-efficient for optimal placement solutions. The basic principle of Crossover and Mutation in GA was incorporated with this proposed system.

Now a daythe feature size of the integrated circuit is shrinking, hence the problem of the integrity is mainly based on the wire length between each and every module in the IC so the Ant Colony Optimization Technique is used for routing in the paper [3]. And here the travelling sales problem is solved efficiently when compared to the other algorithms. In this paper the NP wire problem is solved and the speed is achieved using improved algorithm.

Hybridization of Harmonic Search with Particle Swarm Optimization [4] is used to reduce the temperature produced by the number of modules in the Integrated Chip. It performs well with the more number of modules with less area and less wirelength. The modified corner list(MCL) algorithm was used for representing the modules with less computational complexity.

In this paper [5] Discrete FireFly algorithm is proposed for the circuit partitioning in physical design of VLSI. Mostly, The CAD industries facing the problem of time to market and quality of the chip due to the increasing size of transistor on every 18 months. To overcome those types of problem DFACP is proposed to improve the speed in the each and every module of the design.

The first step of physical design in VLSI is floorplanning, In this paper floorplanning [6] is achieved by hybrid Ant colony and PSO. The main consideration of this work is location of each module in the chip, area occupation, wire length and performance. Two or more modules were floorplanned without overlapping each other. In this paper they introduce some ability of ACO to the PSO to achieve Performance and to reduce the deadspace of the IC.

In this paper abstraction of macrocell overlap is achieved by PSO [7]. PSO with the macrocell placement and overlap abstraction is used to obtain the optimal and better solution for the hard IP placement and enhance its competency to locate solution space as well.

Complex combinatorial problem is solved by using swarm intelligence of FireFly algorithm [8]. This algorithm is basically from the fireflies. The fitness values of fireflies are "the high intensity of light produced on its body" will attract the partner firefly to move towards. In the proposed system routing is achieved with less time delay and wire interconnection.

In this work Ant Colony Optimization [9] was used for the Non-Slicing Floorplanning and it defines the "interior" structure for a geometrical computation of the module positions in the floorplan. The updated ACO reduces the deadspace and wirelength of the integrated circuit.

Craziness predicated Particle Swarm Optimization (CRPSO) is proposed in this paper [10] to expedite the local search and enhances the precision of the chip and to optimize the area and the wirelength interconnections between the modules. The 3rd order IIR filter is utilized for floorplanning demonstration based on CRPSO technique.

Constraint graph of directed acyclic graph is used for Overlap free placement in the Integrated circuit. It provides feasible placement from the relative placement. Then each ant in the colony generated the placement on relative position and provides feedback information about previous colonies. This approach [11] removed the microcell overlap of the horizontal and vertical axis of the module.

In this paper [12], the proposed system is based on window based peak power module which is incorporated with Particle Swarm Optimization technique to select the test rectangles of cores in the system-on-chip (SOC). The Soc benchmarks are proposed to identify the exact thermal effects of the cores at the time of scheduling test.

In this proposed system FireFly evolutionary algorithm [13] was compared with the Artificial Bee Colony algorithm (ABC). The better solution for the set of Minimal Rectilinear Steiner Tree (MRST) is produced by the FireFly algorithm. Delay in the transmission of signals due to resistive, capacitive or inductive wire interconnects. Sometimes, the interconnect having the fixed area and flexible length, then the length of the wire can be minimized for the optimal routing.

SUMMARY TABLE

Ref Number	Optimization Techniques	Area & speed	Wire length and interconnections	Temperature
1	Ant Colony Optimization Technique in Evolutionary algorithm	Area Optimization rate is 90% good and has the error 10%. Running Time of combined Optimization is 33m with 0% error.	It is moderate when compared to other algorithm.	$\triangle$Tmax was optimized to 7.8◦C or 14.6◦C.
2	Particle Swarm Optimization Technique which was incorporated by GA mutation and Crossover.	The area of proposed algorithm for apte is 46.92 mm^2, Xerox is 20.38 mm^2 and ami33 is 1.29mm^2 in MCNC circuits.	Wirelength of apte is 263m, Xerox is 477mand ami33 is 69m in MCNC benchmark circuits.	-
3	Basic Ant Colony Optimization Technique to solve Travelling Salesman Problem.	Area minimization is the main goal. Delay will be reduced up to 75%.	Multi-terminal wiring is achieved with better solution.	Temperature was less when compared to simulated annealing.

4	Hybrid Particle Swarm Optimization and Harmonic Search Algorithm.	Modified Corner List algorithm is used to represent the fitness value for area of each particle.	Wirelength is reduced drastically when compared with genetic algorithm.	Hotspot tool is integrated with HPSOHS for determining temperature.
9	Hybrid Ant colony and Particle Swarm Optimization PSO.	ACO is used for positioning each modules to optimize area	Combined ACO and PSO has less wirelength than PSO	_
10	Craziness based Particle Swarm Optimization algorithm	IIR filter is utilized to minimize the area .Area minimization is more optimized than PSO.	Estimation parameter of wire length is less than PSO.	Thermal aware of proposed system is moderate.

CONCLUSION

Physical design of VLSI floorplanning is a NP hard optimization problem in VLSI chip. Many evolutionary algorithms are used to obtain the feasible solution. The performance and function of the chip is determined by the benchmark circuits. The benchmark circuits such as MCNC benchmark circuit and GSRC benchmark circuit. The representation algorithms are used to represent the modules with flexibility and less computational complexity. For the better results of multi objective floorplan Particle Swarm Optimization Technique are employed.

REFERENCES

[1] RongLuo and Peng Sun, Third International Conference on Natural Computation of IEEE,2007; Vol:04,pp: 751-755.

[2] Guolong Chen, Wenzhong Guo and Yuzhong Chen, Journal of s of computing – A fusion of Foundations, Methodologies and Applications, 2010; vol:14, pp:1329- 1337 .

[3] Han Liying, Tang Hongmei,Sun Zhijie, Zhang Cunshan and Zhao Hongdong. International Conference on Computer and Communications Security,2009; pp: 44-47.

[4] Sivaranjani Paramasivam, Senthilkumar Athappan, Eswari Devi Natrajan and MaheswaranShanmugam, Circuits and Systems,2016; vol:7, pp:562-573.

[5] Pradip Kumar Sharma and ManinderKaur, International Conference on Electronics and Communication System (ICECS), 2014.

[6] PrabhjitKaur. International Journal for Research Applied Science and Engineering Technology, 2011; Vol:2,pp:473-477.

[7] Sheng-Ta Hsieh, Cheng-Wei Lin and Tsung-Ying Sun, IEEE Swarm Intelligence Symposium, 2005; pp:177-180.

[8] NasirAyob M, Fariz Hassan, Halim Ismail A, Hassan Basri H and SafwanAzmi M, IEEE symposium on computer application and electronics(ISCAIE), 2012; pp:43-47.

[9] Mirzakhmet SYZDYKOV, Madi UZBEKOV, Olympiads in Informatics,2015;Vol:9, pp193–203.

[10] Maji K B, AtreyeGhosh Kar R, MandalD and Ghoshal. B.P, International Conference on Science and Technology,2015; pp:248-253.

[11] StelianAlupoaei and SrinivasKatkoori, IEEE Transactions on Very Large Scale Integration (VLSI) Systems,2004;vol:12,pp:1118-1122.

[12] RajitKarmakar and Santanu Chattopadhyay, International Conference on VLSI Design, 2006; pp:475-480.

[13] Abhinandan Khan, Pallabi Bhattacharya and Subir Kumar Sarkar,Advanced computing Networking and informatics,pp189-197,2014.

[14] Shinn-Ying Ho, Shinn-Jang Ho, Yi-Kuang Lin, and William Cheng-Chung Chu, IEEE Transaction on Very Large Scale Integration (VLSI) system,2004; vol:12.

[15] HandaK, KugaS, IEEE Conference on Evolutionary Computation, 1995; vol:2,pp: 716–721.