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A Survey Onlow Power With High Performance Hybrid Full Adder.

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ABSTRACT

As transistor size scale down and high levels of integration rises, leakage power has turned into an imperative drawback in low-power VLSI technology. This is regularly valid for ultra-low-voltage (ULV) circuits. A fundamental normal combinational advanced circuit is adder. Adders are imperative parts in video processing, image and signal processing applications. So it is vital to have dense, low power adder design for these application fields. In this paper, we have shown multiple approaches for adder. Each technique has unique merits like less power, high speed, and minimized area. Full adder can design using various standard CMOS logic families. These low power circuit designs used to build high speed real time applications like DSP (Digital Signal Processing) in low power.

Keywords: Leakage power, Full adder, CMOS logic families, Digital Signal Processing

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INTRODUCTION

Increasing the portable devices turns to design little zone with high speed. Along these lines, circuits with low power utilization turn into the real contender for configuration of microchips and framework segments. An originator is confronted with more limitations, for example, fast less spacing, and less power utilization. For this reason fabricating high speed basic adders are incredible interest. Distinctive rationale styles tend to support the achievement of one execution perspective to the detriment of others.

Full adder design using various logics PTL, TG, GDI logic, GDI with hybrid CMOS style circuit (MUX based and XOR-XNOR based), Majority based circuit, and Minority function with CMOS bridge style and etc. are talked about in the paper.

DIFFERENT LOGIC TECHNIQUES

THE TRANSMISSION GATE BASED ADDER

The full adder design has TFA [1, 2,6] and TGA [6, 7, 10]. Parallel connection of PMOS and NMOS comprises the TG logic. This causes less drops in voltage but needs double the number of transistors. TG based XNOR and XOR gate design is better than all other design [1–3, 9].Primary hindrance of this rationale type is less driving capacity. Whenever cascadingthis two different styles, it require additional buffer to improve driving capability. It turns to increases the amount of transistors[1] and power.

COMPLEMENTARY PASS TRANSISTOR BASED ADDER

Presence of NMOS PTL with output inverters are the features of CPL logic [4].CPL utilizes 32 transistors with the logic of swing restoration. CPL has essential contrast with pass-transistor. The source terminal is associated with input signals. When the transistor gates are larger than average an issue, which is over-burdening the sources of input happens and makes high capacitance values. CPL and CMOS technologies have these types of problems. Drop in voltage is an inborn issue of Pass-transistor logic.So it needs additional transistors to overcome this issue. But, comparatively CPL is better than CMOS.

GDI BASED ADDER

The GDI (Gate Diffusion Input) [15] strategy appeared in Fig.1 and different functions appeared in table 1. For first look, the fundamental GDI remember the static CMOS inverter; but it has some critical contrasts.

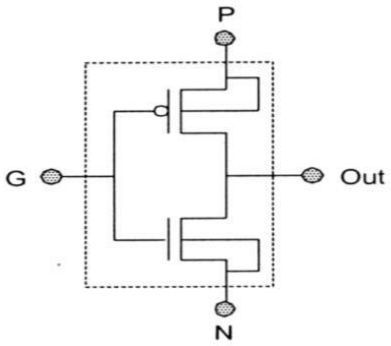

Fig 1: GDI basic cell.

1) GDIhave three types of input sources: 1. Common Gate input for both transistors. 2. P input. 3. N input.
2) Substrate of both transistor associated with source or drain

SOI or twin-well CMOS technologies are more suitable to implement this GDI based gate than P-well. But it is less complex than above techniques.

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N	P	G	Out	Function
0	B	A	A B	F1
B	1	A	A +B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	A B+AC	MUX
0	1	A	A	NOT

Table 1: Different Logic Functions of GDI Cell

GDI BASED ADDER

Really, GDI (an additionally TGDI) logic is some sort of PTL logic yet primary distinction is that in conventional PTL or TG logic. The top-down logic design is so complex, which counteracts generation of basic and all inclusive cell libraries with these logics [15]. GDI logic is appropriate for design of high speed, less power circuits and less count in transistors, while enhancing static power attributes and permitting basic top down design by utilizing small cell library [1, 16].

But in this logic, output swing is decreased for some input combinations. Therefore, additional buffers are needed to solve this issue which in turn expands power utilization [2, 17]. So an upgraded rendition of the GDI logic family called transmission gate diffusion input (TGDI) logic is presented, in which the decrease of output voltage swing has been settled without an additional buffer stage. Expository articulations of GDI logic have been talked about in [8]. In this segment we concentrate on contrasts amongst TGDI and GDI logics. The primary favorable position is the symmetric structure of TGDI logic for P and N inputs. Simulation consequences of delay and power consumption for different inputs in both GDI and TGDI logics are appearing in Table 2. This table proposes that various functions (for various P/N inputs) can be executed with the same delay and power consumption in TGDI logic. In this way, as appeared in Fig. 2, it is conceivable to examine just the upper portion of TGDI cell and extend its results of the whole circuit.

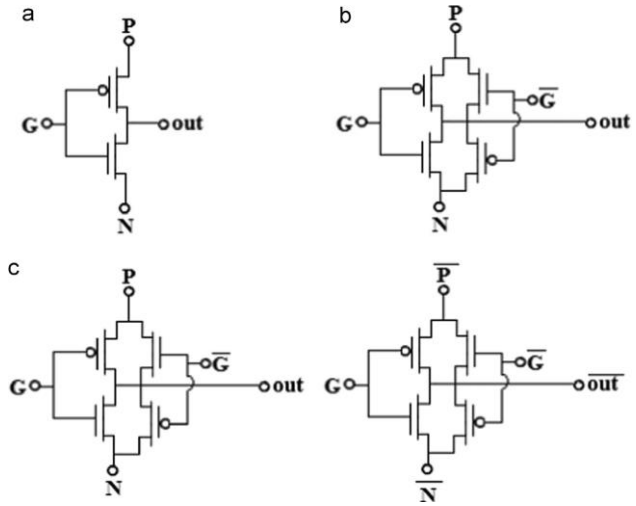

Fig 2: (a) GDI cell. (b) TGDI cell. (c) TGDI cell (with complementary outputs).

input→out	TGDI		GDI	
	Power (nW)	Delay (nS)	Power (nW)	Delay (nS)
P→out	4.94	0.38	3.4	2.13
N→out	4.94	0.38	3.6	1.71
G→out	6.15	0.38	4.4	3.0

Table 2: Comparison delay and power of TGDI and GDI logics for different input and output

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A HYBRID CMOS STYLE BASED ADDER

Combination of more than one logic style called hybrid[11]. Fig.3 one of the example of this style. It has three different modules. The first module uses CPL logic additional with one not gate. High mobility NMOS transistors make these circuits as fast but it takes more power for this circuit operation. The second module composed by TG and normal CMOS gates. Utilization of PMOS directly affects size of the design, and the driving capability also affected by transistors connected in series which causes high power usage. Third module have invertor and normal TG leads less driving ability uses more power when designing proposed circuits. Module.3 uses transmission gate also have some merits and demerits getting high speed output which discussed above.

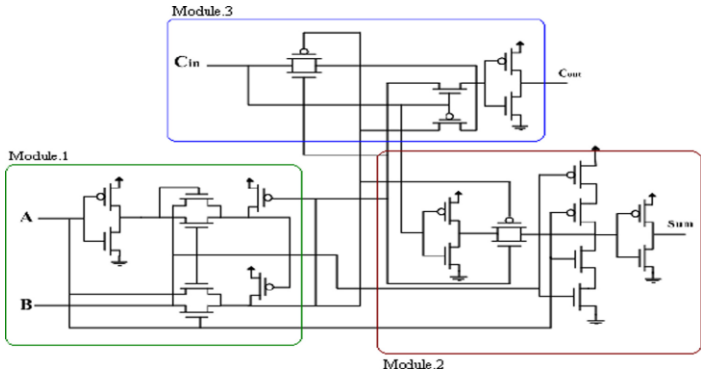

Fig 3: Hybrid Cmos Full adder

DML BASED ADDER

DML (Dual Mode Logic) has been presented as of late as a logic family that can be switched between static and dynamic modes depending upon connecting clock input [18]. DML has higher execution and less power utilization in correlation with standard-static CMOS logic with dynamic and static mode respectively. The conventional DML structure appears in Fig. 4. In DML the M1 transistor and all transistors in pull up or pull down network, which create a parallel path with M1 are intended to have the small size while other transistors in complementary network are measured by standard CMOS logic [19].

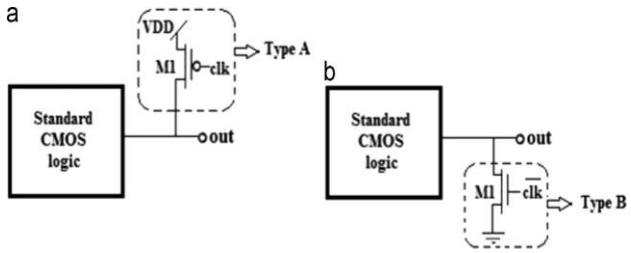

Fig 4: Conventional dual mode logic cell (a) type A, and (b) type B

In static mode, M1 goes off (clk¼VDD) and DML structure is like a standard -static CMOS logic with an additional parasitic capacitance (M1) however utilizing previously mentioned estimating strategy causes the less power utilization. Additionally, in dynamic mode, an asymmetric clock Pre-charging is performed by a small sized M1 transistor and its parallel system goes about as an active keeper, which gives more power in correlation with domino logic [19], furthermore reduces a few disadvantages of domino logic, for example, crosstalk noise, charge sharing and sensitivity to glitches [18].

DUAL MODE TGDI (DMTGDI) BASED ADDER

By utilizing dynamic logic, similar to domino, execution of digital circuits can be viably improved, bet high sensitivity of dynamic logics to process varieties, makes them unacceptable for Nano scale technologies.

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By supplanting CMOS circuit with TGDI in DML structure DMTGDI logic is acquired by fig.5. Utilizing this structure, one may execute an extensive variety of logic function with a couple of transistors in the unit cell.

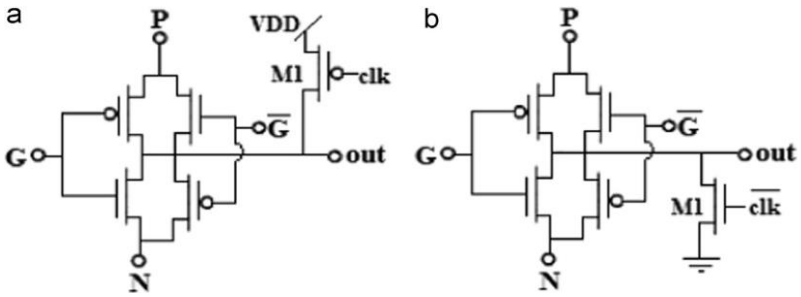

Fig 5: Dual mode logic with TGDI logic cell (a) type A, and (b) type B

In the first place by supplanting pass transistors on GDI logic with transmission gates in TGDI and afterward by changing DML logic based on the TGDI unit cell. Simulation results demonstrate that this logic family has predominant execution and less energy consumption both in subthreshold or more subthreshold regions contrasting with ordinary DML and GDI logics, while acquires flexibility of DML and low energy consumption of GDI. Execution of adder in DMTGDI logic may be enhanced by strategies for DML [16]. Likewise, add up to power utilization can be diminished by setting gates on the critical path in dynamic mode and setting whatever remains of the circuit in static mode [16, 17].

THE MAJORITY-NOT GATE BASED ADDER

The majority based full adder circuit uses bridge style [12, 13]. It also includes the design constrains of less complexity, less power utilizations. This sort of design made with basic CMOS inverter and capacitors. Fig 6 illustrates the strategy of this design. When the majority of input is “0”, Vdd is the output after the inverter operation. Likewise if it is “1”, the output is 0v. MOScap, MIM, PIP capacitors are feasible alternatives to implement the capacitor. PMOS capacitor is chosen for implementing the capacitor network. This design (Fig. 7) has 12T. Table.3 shows the majority function implementation. The selection logic is mag(a,b,c,cbar,cbar).

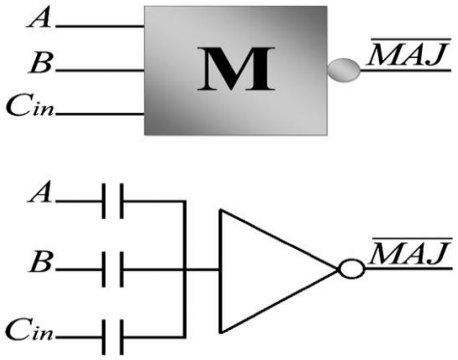

Fig 6: 3-input majority-not gate

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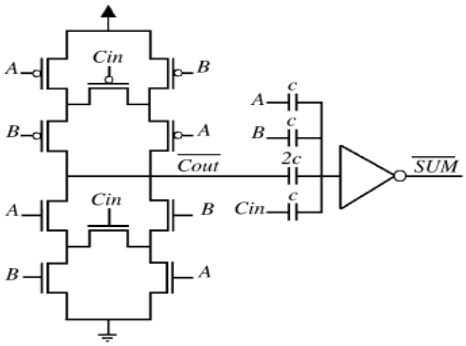

Fig 7: The majority not-gate based, full adder circuit

Functionality of 1-bit Full-Adder

A	B	C_{in}	$\overline{C_{out}}$	MAJ (A, B, C_{in}, $\overline{C_{out}}$, $\overline{C_{out}}$)	Sum
0	0	0	1	0	0
0	0	1	1	1	1
0	1	0	1	1	1
0	1	1	0	0	0
1	0	0	1	1	1
1	0	1	0	0	0
1	1	0	0	0	0
1	1	1	0	1	1

Table 3: Majority gate function

CONCLUSION

Due to the rapid growth of portable devices, designing low power, high performance devices are more important. This paper gives the exposure about design of optimized full adder. Based on the design constraints (Low power, area, high, speed) any one (or more) technology chosen. By this proposed adder designer can build a full adder based circuits like multiplier for the real time applications of DSP.

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