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Review on Performance of Multipliers.

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ABSTRACT

The elaboration in VLSI design with an increase results decrease/increase on major factors like Power, area, and speed. A multiplier has an important role in a mixture of arithmetic operations in digital processing applications. By means of progression in operating frequency, semiconductor technology, chip density are increasing, and results usage of power consumption in VLSI circuits has become a major problem of kindness. Fast growing technology has raise demands for high-speed and efficient real time DSP applications. A more number of multipliers design have been developed to improve their speed. A study on various multiplier techniques are observes in this paper.

Keywords*:* Binary Multiplier, Array Multiplier, Wallace Tree Multiplier, Abacus Multiplier.

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INTRODUCTION

In the design of systems using DSP and further applications multiplier is an important basic building block. Several research scholars are continuously trying to design multiplier with low power consumption, high speed, normal structure, such that it will occupies less area for compact VLSI implementation. A numerous types of algorithms are proposed in the earlier period to perform multiplication operation process. Each algorithms have it significant role in performing multiplication operation and results its own advantages and having trade-offs between themselves by means of circuit complexity, power, speed and area. The main aim of this paper is as follows: Section II deals about literature survey. In this section an introduction to Binary Multiplier, Wallace Tree Multiplier, Array Multiplier, Abacus Multiplier is presented.

Different Multiplier Techniques

Binary Multiplier: The most commonly known and easiest multiplication method is binary multiplication. For example, let us consider a normal four by four bit multiplication is shown below. A normal multiplication of multiplier and multiplicand results a partial product value as shown below.

11 X 13 = 143.

11= (1011)
X = 143(10001111)
13= (1101)

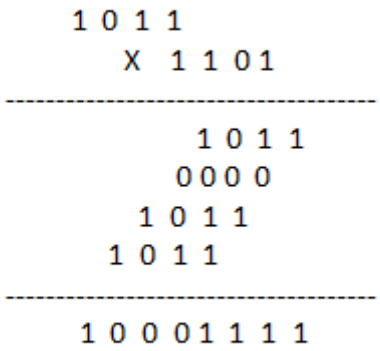

Fig 1: Binary Multiplication

The above multiplication algorithm is the easiest form but for more number of bit size it is too complex.

Array Multiplier: An array multiplier two binary numbers will be multiplied by using of an array of full adders and half adders. At the same time addition of the distinct product terms is done in this array multiplier [1]. An array multiplier orginates from the multiplication parallelogram as shown in below fig 2. In this each stage of the parallel adders will gets some partial products inputs. The carry output is propagating to the next row one of the input. The bold line indicates in the below figure is the major role of multiplier. In a non pipe-lined array multiplier, the partial products will generate at the same time. It shows that a major part consists of two types i.e., vertical and horizontal. Both have same delay in terms of full adders and gate delays. For example a NXN – bits array multiplier, the vertical and horizontal delays are both the same the delay of an n-bit full adder.

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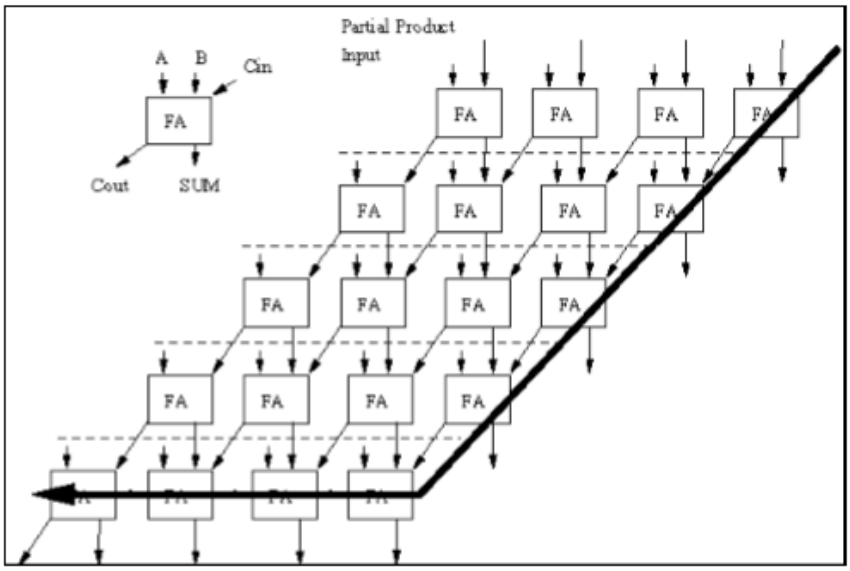

Fig 2: A 4X4 bits Array Multiplier

The gain of an array multiplier is that it has a regular structure. An additional advantage of the array multiplier is easy of design for a pipelined architecture. Major limitation of array multiplier is its size. As operand sizes increase, arrays grow in size at a rate equal to the square of the operand size. It comes under conventional multiplier.

Wallace Tree Multiplier (WTM): One of the recent most used multiplier technique used in now a days is WTM.Wallace tree multiplier is an efficient hardware implementation of a digital circuit to facilitate multiplies of two integers. Wallace trees are asymmetrical structure in that the informal picture does not specify a regular method for the compressor interconnections.

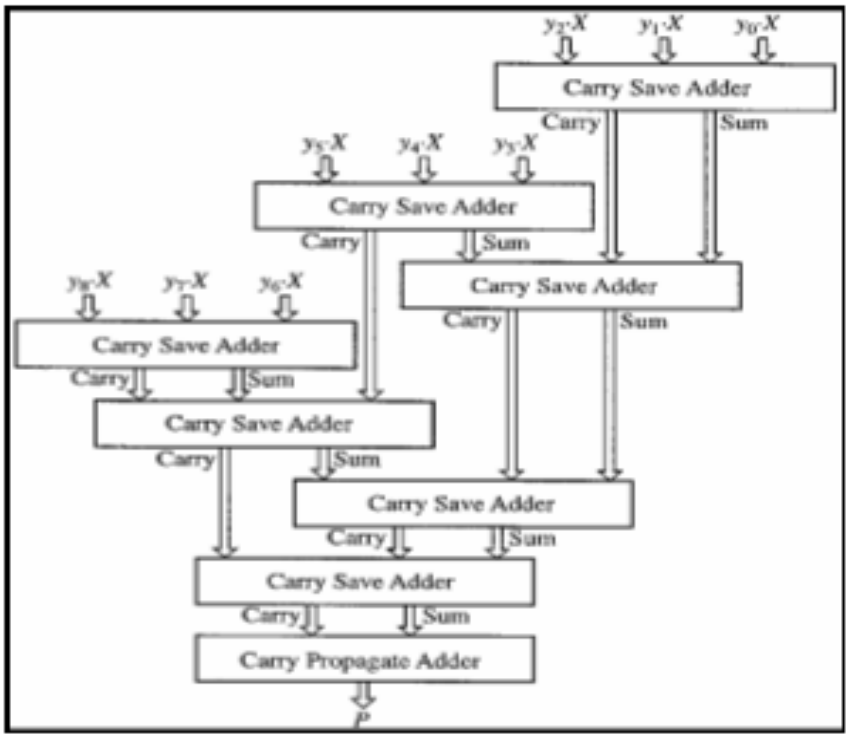

Fig 3: Wallace Tree Multiplier

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Although still it is an efficient implementation of adding partial products (PP) in parallel. This method is carried out in three steps i.e. after the completion of multiplication operation the addition step is carried out in different format that is the resulted rows additions can be done through the column compression logic.

Wallace Tree Multiplier uses only Full and Half Adders. Wallace tree multiplier method is to decrease the no. of adders by minimize the number of the half adder in any multiplier [2]. The first partial product is the least significant bit (LSB) in the output of the multiplier result. After that, moving to the next column of the partial product if there are any adders from the previous product, the full Adder is used otherwise a half adder is used.

Booth Multiplier: An answer for realizing the high speed multipliers is to enhance parallelism which helps in reduce. The original version of Booth's multiplier (Radix – 2) had two drawbacks. The number of add / subtract operations became variable and hence they became inconvenient while designing Parallel multipliers. The Algorithm becomes inefficient when there are isolated 1s. These problems are overcome by using Radix 4 Booth's Algorithm which can scan strings of three bits

An 8-bit booth multiplier [4] needs only four partial products to be added instead of eight partial products generated using conventional multiplier. The architecture design for the modified Booths algorithm used in this design is shown in fig 4.

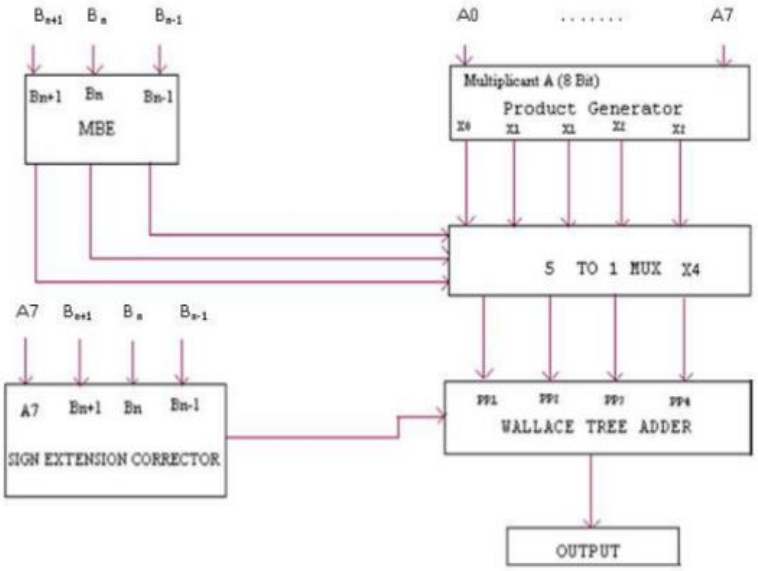

Fig 4: Booth Multiplier

In order to achieve high-speed multiplication algorithms using parallel counters, the modified Booth algorithm and some multipliers based on the algorithms have been implemented for practical use. This type of multiplier operates much faster than an array multiplier for longer operands because its computation time is proportional to the logarithm of the word length of operands.

Abacus Multiplier: The ABACUS multiplier implementation has parallel counters that make a decision on the position of carry. While parallel counter approach does not require a separate column-wise compression, the realization may combine the compression and carry cycles. The architecture intends of an abacus multiplier primarily uses full adders to compute addition of second and third bits. As an answer, the first, second and third columns don`t need any parallel counters for addition. Additional columns with more than three elements need parallel counters to transmit carries to the next stage. A multiplier in this structure result of consisting a various stages of full adders, either stand-alone or within parallel counters, each stage adding up to the total delay.

The 4 bit abacus multiplier design shown in the below fig.5, the first stage of architecture, seven full adders are used, three of which are for the (4, 3) parallel counter. The second stage uses five full adders, and

finally last stage requires only two full adders to generate the result. Which come close to minimizes carry operations and results in reduce in delay.

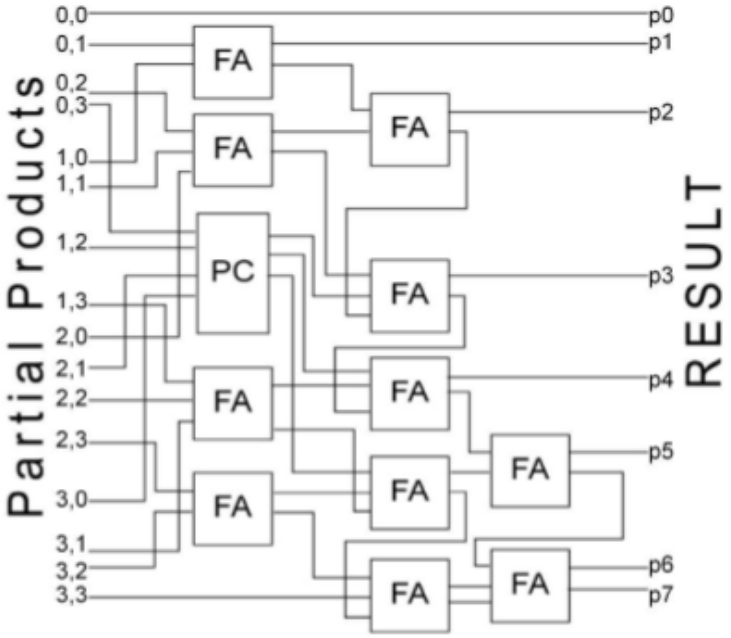

Fig 5: A 4 bit Abacus Multiplier

CONCLUSION

In this study, a feasible logic implementation is introduced for ABACUS multiplier architecture for the first time and compared with different multipliers techniques. Based on the extensive survey abacus multiplier performance is best compare to the other multipliers.

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